REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion, is respectfully requested.

Claims 1, 2, and 5-20 are currently pending. No claim amendments are presented, thus, no new matter is added.

In the outstanding Office Action, Claims 1-5, 10-13, and 18-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Saito (U.S. Pub. No. 2002/0026553) in view of Texas Instruments ("Product Bulletin: Boundary-Scan Logic," hereafter "TI-BSL"); Claims 6-9 were rejected under 35 U.S.C. §103(a) as unpatentable over Saito in view of TI-BSL and Kumiko (Japanese Patent No. JP-9064811); and Claims 14-17 were rejected under 35 U.S.C. §103(a) as unpatentable over Saito in view of TI-BSL and Edwards et al. (U.S. Patent No. 6,684,348, hereafter "Edwards").

Applicants thank the examiner for the courtesy of an interview with Applicants' representative, Mr. Sameer Gokhale, on May 28, 2009. During the interview, the differences between the claims and the applied art were discussed. The examiner clarified his interpretation on how he believes the applied art discloses certain features of Claim 1. The Applicants' representative explained what were believed to be deficiencies of the applied art with regard to Claim 1. No agreement was reached, and the examiner indicated he would further consider the Applicant's arguments upon submission of a formal response. Arguments similar to those presented during the interview are presented below.

With respect to the rejection of Claim 1 under 35 U.S.C. §103(a), Applicants respectfully traverse this ground of rejection. Claim 1 recites, *inter alia*,

> a plurality of function blocks configured to perform signal processing, each function block comprising one or more devices which collectively perform a specified function of the signal processor;

> a plurality of dedicated paths configured to transmit debug information for debugging the signal processor, the debug information obtained from respective function blocks of the plurality of function blocks;
>
> a selection multiplex output block connected to the plurality of dedicated paths and configured to input the debug information via the dedicated paths, and output the inputted debug information;
>
> a processing unit configured to transmit an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block; and
>
> at least two of the dedicated paths are provided to connect the at least one of the function blocks with the selection multiplex output block such that the selection multiplex output block has at least two inputs from the at least one of the function blocks, said at least two of the dedicated paths configured to transmit input data and output data associated with the at least one of the function blocks, as the debug information, from the at least one of the function blocks to the selection multiplex output block in response to the instruction from the processing unit.

Applicants respectfully submit that the combination of Saito and TI-BSL fails to disclose or suggest at least these features of Claim 1.

Saito describes a method for monitoring regions in a processor circuit for bugs. Saito shows in Figs. 4-9, and 11 that functional blocks 21 send and receive signals outside the circuit through selection means 30 or through signal selection circuit 32 (see para. [0032] of Saito). Saito also describes a processor circuit 1 in Fig. 4, and at least one MPU Core 1 in Figs. 5-9, and 11. Saito describes the processor circuit or the MPU Core can send and receive signals to the plurality of functional blocks 21 (see para. [0031] and [0038]).

The Office Action acknowledges that Saito fails to disclose or suggest "at least two of the dedicated paths provided for one of the plurality of function blocks, said paths configured to transmit input data and output data associated with said one of the plurality of function

blocks, as debug information from said one of the plurality of function blocks to the selection multiplex output block." (See Office Action at pages 3-4).

However, Applicants submit that the full deficiency of Saito is that it fails to disclose or suggest "at least two of the dedicated paths are provided to connect the at least one of the function blocks with the selection multiplex output block ***such that the selection multiplex output block has at least two inputs from the at least one of the function blocks***, said at least two of the dedicated paths configured to transmit input data and output data associated with the at least one of the function blocks, as the debug information, from the at least one of the function blocks to the selection multiplex output block in response to the instruction from the processing unit," as defined by Claim 1.

Furthermore, the Office Action has not explicitly addressed whether or not Saito discloses "a processing unit configured to transmit an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block," as was added in the previously filed amendment to Claim 1.

Saito describes that the processor circuit or the MPU Core can send and receive signals to the plurality of functional blocks 21 (see para. [0031] and [0038]). However, Saito never describes that the processor circuit 1 or the MPU Core 1 transmits an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block.

Therefore, Applicants respectfully submit that Saito fails to disclose or suggest "a processing unit configured to transmit an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block," as defined by Claim 1.

The Office Action relies on TI-BSL to remedy the deficiencies of Saito with regard to Claim 1. (See Office Action at pages 3-4).

TI-BSL is directed towards boundary-scan logic technology. The figure shown on page 3 of TI-BSL shows a core logic unit that is to be tested within the boundary-scan architecture. Boundary-scan register cells (BSCs) are interconnected between input/output pins and the core logic unit (see page 3 of TI-BSL, sixth full paragraph). During normal operations, input and output signals pass freely through the BSCs from a normal data input to the normal data output. When boundary test mode is entered, the BSCs operate to allow test stimulus data to be input from the test data input (TDI) pin and into the core logic unit and output to the test data output (TDO) pin. Thus, the BSCs create an architecture that allows bypassing of normal input/output signals so that test stimulus data can be transmitted through the core logic unit and output to the TDO for inspection.

The previous amendment to Claim 1 defined "a processing unit configured to transmit an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block," ***and*** "at least two of the dedicated paths are provided to connect the at least one of the function blocks with the selection multiplex output block ***such that the selection multiplex output block has at least two inputs from the at least one of the function blocks***."

The Office Action takes the position that there is a dedicated scan path through each BSC, and therefore it appears that the examiner interprets at least two of these separate scan paths through respective two BSCs correspond to the claimed "at least two of the dedicated paths." Furthermore, the Office Action indicated that that the multiplex operation of an individual BSC may constitute the claimed "selection multiplex output block." However, Applicants submit that the Office Action has not shown that a multiplex function of an individual BSC "***has at least two inputs from the at least one of the function blocks***," **and**

that at least two of the dedicated paths transmit input data and output data from the function block to an individual BSC multiplexer in response to the instruction from the processing unit.

The Office Action takes the position that a multiplexer connected to the end of the boundary scan chain (i.e., the boundary scan register) may constitute the claimed "selection multiplex output block." However, the multiplexer shown at the end of the boundary scan register is only shown to receive one input from the last BSC at the end of the boundary scan register, and thus is only shown to receive one input from the core logic unit (as a function block). Therefore, the multiplexer shown at the end of the boundary scan register does not correspond to the claimed "selection multiplex output block" which "has at least two inputs from the at least one of the function blocks," as defined by amended Claim 1.

During the interview, the examiner also discussed that the BSCs of the boundary scan register can be interpreted as being the "selection multiplex output block because they selectively pass data from BSCs that are earlier in the scan path (see also Office Action, at pages 4-5).

However, as discussed above, Claim 1 also defines "a processing unit configured to transmit an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block." As discussed above, it does not appear that the Office Action explicitly addresses this feature which was added in the Applicants' previous amendment.

TI-BSL appears to show that an instruction comes from the TDI pin (see pages 4-5) and flows through the BSCs in the boundary register to instruct the BSCs on how to operate. However, TI-BSL does not show that a processing unit transmits an instruction to the core logic unit instructing it to transmit the input and output data as debug information to a selection multiplex output block. On the contrary, TI-BSL shows that the core logic unit (as

a function block) is insulated from the actual instructions associated with the boundary scan register. Therefore, if the examiner interprets the boundary scan register as the "selection multiplex output block" and thus external to the claimed function block, then TI-BSL does not disclose the feature of "a processing unit configured to transmit an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block," because as discussed above the actual core logic unit itself does not receive such an instruction.

Additionally, if the examiner interprets that the boundary scan register is part of the claimed "function block" and is receiving an instruction to transmit input and output data as debug information, then the boundary scan register cannot also be the claimed "selection multiplex output block" as asserted in the Office Action.

Therefore, Applicants submit that TI-BSL fails to disclose or suggest all of "a processing unit configured to transmit an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block," ***and*** "at least two of the dedicated paths are provided to connect the at least one of the function blocks with the selection multiplex output block such that the selection multiplex output block has at least two inputs from the at least one of the function blocks, said at least two of the dedicated paths configured to transmit input data and output data associated with the at least one of the function blocks, as the debug information, from the at least one of the function blocks to the selection multiplex output block in response to the instruction from the processing unit," as defined by Claim 1.

Thus, Applicants respectfully submit that TI-BSL fails to remedy the deficiencies of Saito with regard to Claim 1.

Thus, Applicants respectfully submit that Claim 1 (and all associated dependent claims) patentably distinguishes over Saito and TI-BSL, either alone or in proper combination.

Kumiko and Edwards have been considered but fail to remedy the deficiencies of Saito and TI-BSL with regards to Claim 1.

Therefore, it is respectfully submitted that Claim 1 (and all associated dependent claims) patentably distinguish over Saito, TI-BSL, Kumiko, and Edwards, either alone or in proper combination.

Consequently, in light of the above discussion, the outstanding grounds for rejection are believed to have been overcome. The present application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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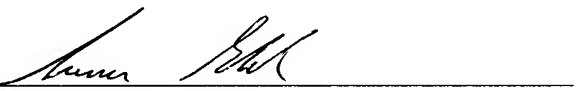

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